CLAIMS

What is claimed is:

1. A process for fabricating a complementary metal oxide semiconductor (CMOS) structure comprising:

providing a plurality of polySi gates overlying a semiconductor substrate, each polySi gate comprises a dielectric cap located on an upper surface thereof;

forming silicided source/drain regions in the semiconductor substrate;

forming a planarized dielectric stack on the semiconductor substrate;

performing an etching process to expose an upper surface of each polySi gate; and

performing a salicide process which converts each polySi gate to a metal silicide gate, wherein each metal silicide gate has substantially the same height, is composed of the same silicide phase, and has substantially the same workfunction for the same polySi ion implant conditions.

2. The method of Claim 1 wherein the plurality of polySi gates are formed atop a gate dielectric.

3. The method of Claim 1 wherein the plurality of polySi gates are formed by deposition, lithography and etching.

4. The method of Claim 1 wherein the dielectric cap is composed of a nitride.

5. The method of Claim 1 wherein the step of providing the plurality of polySi gates includes the formation of at least one spacer on each exposed sidewall of the polySi gates.

6. The method of Claim 5 wherein the at least one spacer includes a first spacer and a second spacer, wherein the first spacer has a thickness that is narrower than the second spacer.

7. The method of Claim 1 wherein the step of forming the silicided contacts on source/drain regions comprises depositing a metal atop the semiconductor substrate, and performing a salicide process.

8. The method of Claim 7 wherein the metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

9. The method of Claim 8 wherein the metal is Co, Ni or Pt.

10. The method of Claim 7 wherein the salicide process comprises a first anneal, a selective etching step and optionally a second anneal.

11. The method of Claim 7 further comprising forming a layer of silicon atop the semiconductor substrate prior to metal deposition.

12. The method of Claim 1 wherein the step of forming a planarized dielectric stack comprises deposition and planarization.

13. The method of Claim 1 wherein the step of forming a planarized dielectric stack comprises forming an etch stop layer, forming an interlevel dielectric and planarizing the interlevel dielectric.

14. The method of Claim 1 wherein the etching process comprises a reactive ion etch step.

15. The method of Claim 1 wherein the salicide process comprises depositing a blanket silicide metal layer atop the at least the exposed upper surface of each polySi gate, first annealing to cause total or partial consumption of the polySi gates, selective etching non-reacted silicide metal and optionally performing a second anneal.

16. The method of Claim 15 wherein the silicide metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

17. The method of Claim 16 wherein the silicide metal is Co, Ni or Pt.

18. The method of Claim 15 the first anneal is performed at a temperature from about 350° to about 550°C.

19. The method of Claim 15 wherein the optional second anneal is performed at a temperature from about 600°C to about 800°C.

20. A CMOS structure comprising;

a plurality of silicided metal gates located atop a surface of a gate dielectric, each of the silicided metal gates is composed of the same silicide phase, has substantially the same height, and has substantially the same workfunction for the same polySi ion implant conditions regardless of the dimension of the silicided metal gate.

21. The CMOS structure of Claim 20 wherein the silicided metal gates comprise a metal selected from the group consisting of Ti, Ta, W, Co, Ni, Pt, Pd and alloys thereof.

22. The CMOS structure of Claim 21 wherein the metal is Co, Ni or Pt.

23. The CMOS structure of Claim 20 further comprising a gate dielectric located between each silicided metal gate and the semiconductor substrate.

24. The CMOS structure of Claim 23 wherein the gate dielectric comprises SiO_2, SiO_xN_y, HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, Y_2O_3, $SrTiO_3$, $LaAlO_3$, silicates or combinations thereof.

25. The CMOS structure of Claim 20 further comprising silicided source/drain regions adjoining each silicided metal gate.

26. The CMOS structure of Claim 20 wherein each silicided metal gate comprises $CoSi_2$, PtSi or NiSi.

27. The CMOS structure of Claim 20 wherein at least one spacer is located on sidewalls of each of the silicided metal gates.

28. The CMOS structure of Claim 27 wherein the at least one spacer includes a first narrow spacer and a second wider spacer.

29. The CMOS structure of Claim 20 wherein the silicide gates include a dopant selected from the group consisting of As, P, B, Sb, Bi, In, Al, Ga, Tl and mixtures thereof, the dopant changes the workfunction of the silicided metal gate.

30. A method of forming a CMOS structure having silicide contacts comprising the step of:

providing a structure comprising a plurality of polySi gates overlying a semiconductor substrate;

depositing a silicide metal atop the structure including the polySi gates and the semiconductor substrate;

forming a recessed, reflow material between each polySi gate;

removing silicide metal from atop each of the polySi gates;

removing the recessed, reflow material; and

annealing the structure so as to form silicide contact regions between each of the polySi gates.

31. The method of Claim 30 wherein the silicide metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

32. The method of Claim 31 wherein the metal is Co, Ni or Pt.

33. The method of Claim 30 wherein the recessed, reflow material comprises an antireflective coating or a spin-on dielectric.

34. The method of Claim 30 wherein the forming the recessed, reflow material comprises deposition and optional etching.

35. The method of Claim 30 wherein the removing the silicide metal comprises a wet etching process.

36. The method of Claim 30 wherein the annealing includes at least a first annealing step which is performed at a temperature from about 300°C to about 600°C.

37. The method of Claim 36 further comprising an optional second annealing step which is performed at a temperature from about 600°C to about 800°C

38. The method of Claim 30 further comprising forming silicide metal gates by depositing and planarizing a capping bilayer comprising SiO_2 and Si_3N_4; performing an optional wet etch process to remove SiO_2; performing a selective RIE process to remove Si_3N_4 atop the gate; forming a silicide metal on the gate; and performing a salicide process.

39. A method of forming a CMOS structure having silicide contacts comprising the step of:

providing a structure comprising a plurality of polySi gates overlying a semiconductor substrate;

forming a bilayer layer comprising a metal-containing layer and a capping layer atop the structure including the polySi gates and the semiconductor substrate;

forming a planarizing material on the semiconductor substrate;

exposing the metal-containing layer atop each polySi gate;

removing the metal-containing layer from atop each polySi gate;

planarizing the planarizing material; and

annealing the structure so as to form silicide contact regions between each of the polySi gates.

40. The method of Claim 39 wherein the metal-containing layer comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

41. The method of Claim 40 wherein the metal-containing layer is Co, Ni or Pt.

42. The method of Claim 39 wherein the capping layer comprises TiN, W or Ti.

43. The method of Claim 39 wherein the planarizing material comprises a photoresist or a low temperature oxide.

44. The method of Claim 39 wherein the exposing comprises chemical mechanical polishing of the planarizing material and etching of the capping layer.

45. The method of Claim 39 wherein the removing of the metal-containing silicide metal from atop each polySi gate includes a wet etching process.

46. The method of Claim 39 wherein the annealing includes at least a first annealing step which is performed at a temperature from about 300°C to about 600°C.

47. The method of Claim 46 further comprising an optional second annealing step which is performed at a temperature from about 600°C to about 800°C

48. The method of Claim 39 comprising forming silicide metal gates by depositing and planarizing a capping bilayer comprising SiO_2 and Si_3N_4; performing an optional wet etch process to remove SiO_2; performing a selective RIE process to remove Si_3N_4 atop the gate; forming a silicide metal on the gate; and performing a salicide process.

49. A CMOS structure comprising:

a plurality of polySi gates located atop a surface of a gate dielectric, each of the polySi gates has substantially the same height, regardless of the dimension of the polysilicon gates and silicided contacts located between each polySi gate.

50. The CMOS structure of Claim 49 wherein the polySi gates include a dopant selected from the group consisting of As, P, B, Sb, Bi, In, Al, Ga, Tl and mixtures thereof.

51. The CMOS structure of Claim 49 wherein the silicide contacts comprise NiSi, $CoSi_2$ or PtSi.

52. The CMOS structure of Claim 49 wherein the silicide contacts are self-aligned with outer edges of a spacer that is located on a sidewall of each polySi gate.